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ADOSE DELIVERABLE D2.5; PUBLIC SUMMARY
'PACKAGING CONCEPT FOR A FIR CAMERA SUBSYSTEM'

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1. TARGET OF DEVELOPMENT

Workpackage 2 of the ADOSE project develops integrated far-infrared (FIR) sensor arrays for hot spot detection in warning night vision systems with NIR / FIR data fusion. New technological approaches for the FIR sensor array with significantly reduced cost are developed and include cost efficient vacuum wafer-level packaging methods. For the final Chip-on-Board (COB) attach of the FIR imager chip a new concept had to be worked out to assure a reliable COB assembly yielding low thermal gradients across the active sensor area.

2. CONCEPT FOR CHIP-TO-BOARD ATTACH

The FIR chip has to convert thermal radiation in the 8-14µm wavelength range from road objects into an electrical signal by detecting the induced temperature change. As this changes are only in the range of a few milli-Kelvin, the sensor array is also very sensitive to temperature changes caused by other internal and external influences. A homogenous and stable temperature distribution for all sensor cells across the array area is essential.
Investigations on the main influences of the chip's temperature gradient have been done and showed that the major influence originates from the internal power dissipation of read-out IC's (ROIC) heating zones in the chip. The environmental temperature, the chassis temperature and thermal radiation falling on the camera box have influence on the absolute chip temperature, however, do not severely change the temperature gradient across the chip.

From simulations of the thermal and the stress situation for different concepts of attaching the chip to the board, a solution has been identified which allows to dissipating the heat from the hot zones in the chip towards the board and the environment. Figure 1 shows two different possibilities of chip attach with either good thermal properties or good reliability. These concepts have been combined into a FIR COB package suitable for both, good reliability and low thermal gradients across the chip.

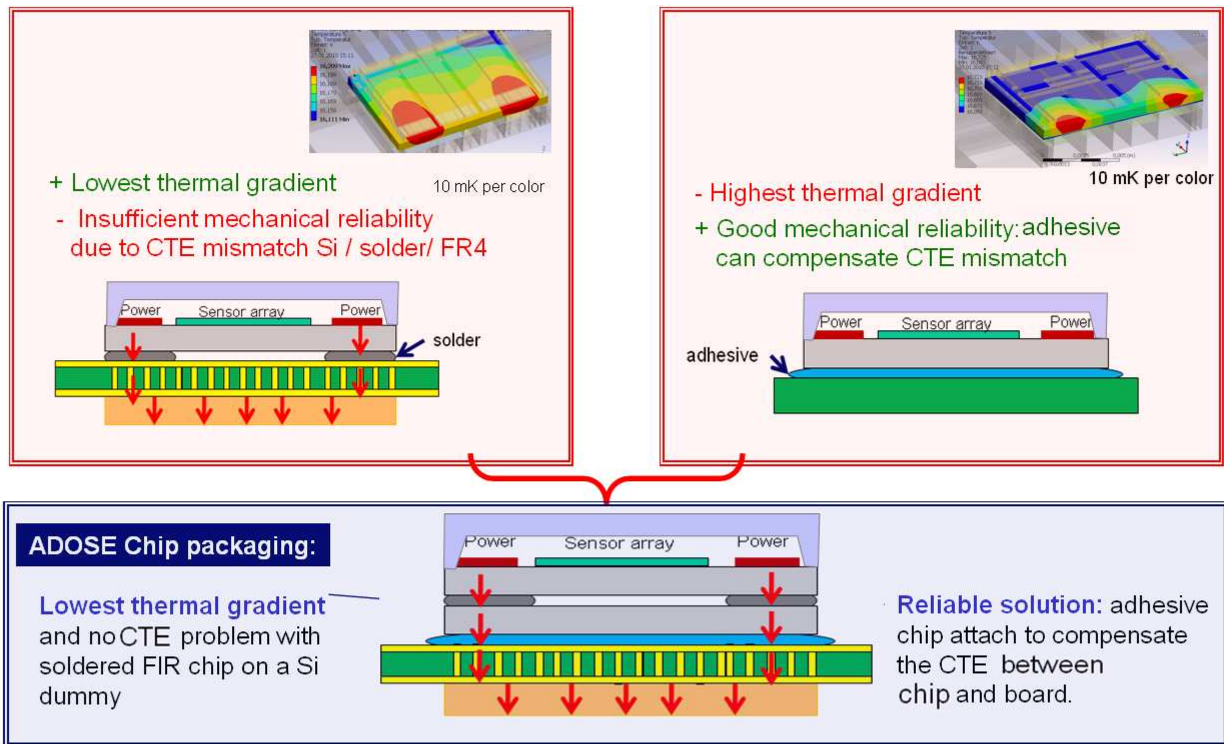

Figure 1: Combination of a thermally optimized chip-to-chip setup with a reliable chip-to-board setup

The FIR-chip is soldered on a piece of silicon acting as a heat spreader where the solder is placed only below those ROIC parts with high power dissipation which are located along the two longer sides of the chip. Heat will preferably flow in a vertical direction to the heat-spreader chip, where it is distributed in a uniform way and then conducted through the adhesive to a heat sink realized in the FR4 board. The sensor part of the FIR chip will heat up a little bit to the temperature of the power part and the thermal gradient in the FIR chip is reduced considerably. In addition the adhesive attach of the double chip allows reducing problems caused by mismatch in the coefficients of thermal expansion (CTE) between silicon and FR4, in order to achieve a good reliability for the chip-to-board bonding technology.

3. DEVELOPMENT OF A COB TECHNOLOGY FOR THE FIR IMAGER CHIP

The rear side of the FIR chip as well as the silicon plate have to be metallised for a partial soldering technology. Sputter metallization layers have been selected and tested on silicon dummies to perform reflow tests. Six different metallization layers were investigated for use with AuSn and SnAg solder alloys. To qualify the soldering compatibility of the dice and the metallization, several soldering tests have been performed. The dice were sheared off after soldering and the metallurgical reaction between solder and metallization were analyzed in cross-sections. The shear tests confirmed the results of the optical inspection of the test assemblies. For only one metallization de-wetting was observed (metallization C) and the shear values were too low. For all other metallizations the shear mode showed chip breakage. Therefore, the solder interface was excellent. Further SEM / EDX analyses proved that no intermetallic phases were built, which could reduce the reliability, even after three sequenced reflow processes.

As the chip and the heat spreader metallizations are not structured, a non standard assembly process had to be developed for partial soldering. An unfilled polymer is used for protection of the array region during soldering of the heat contact using SnAg. Maintaining the exact border between both materials is a critical issue. Measurements of the real dimensions have been made under IR and x-ray microscopy and proved that a sharp border between the polymer and metal interconnect was achieved.

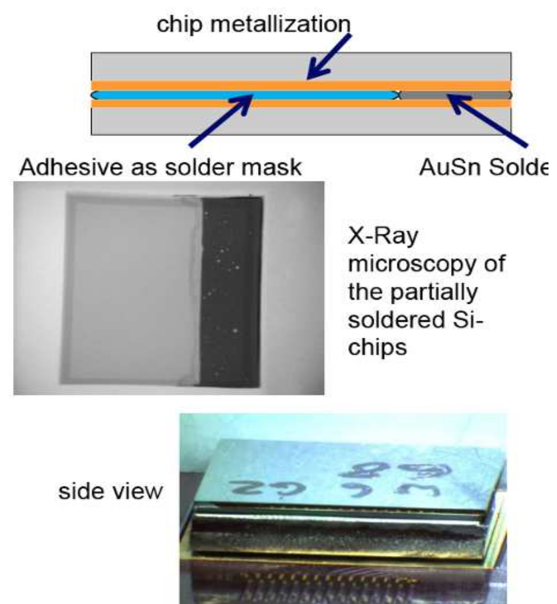

Figure 2: Chip packaging concept experimentally verified with 1st generation test chips

4. INTEGRATION INTO THE FIR CAMERA-DEMONSTRATOR

A camera box (Figure 3, top) for the FIR chip has been designed. In order to avoid interference, it consists of two internal compartments, one for the FIR chip stack mounted on the PCB substrate and another for rest of the camera electronics. Following the FIR packaging concept of ADOSE deliverable 2.5 in meanwhile a first setup of the wafer-level packaged FIR-imager chip attached to a PCB has been realized. In the final camera setup this PCB board carrying the FIR chip together with a few supporting IC's for driving and signal conversion on the rear will be attached directly on the lens assembly with distance holders ensuring the correct focus plane for the FIR chip (Figure 3, bottom). With such COB assembled FIR imager chips more compact and more cost efficient systems can be built than it was possible with previous discrete and expensive FIR packages.

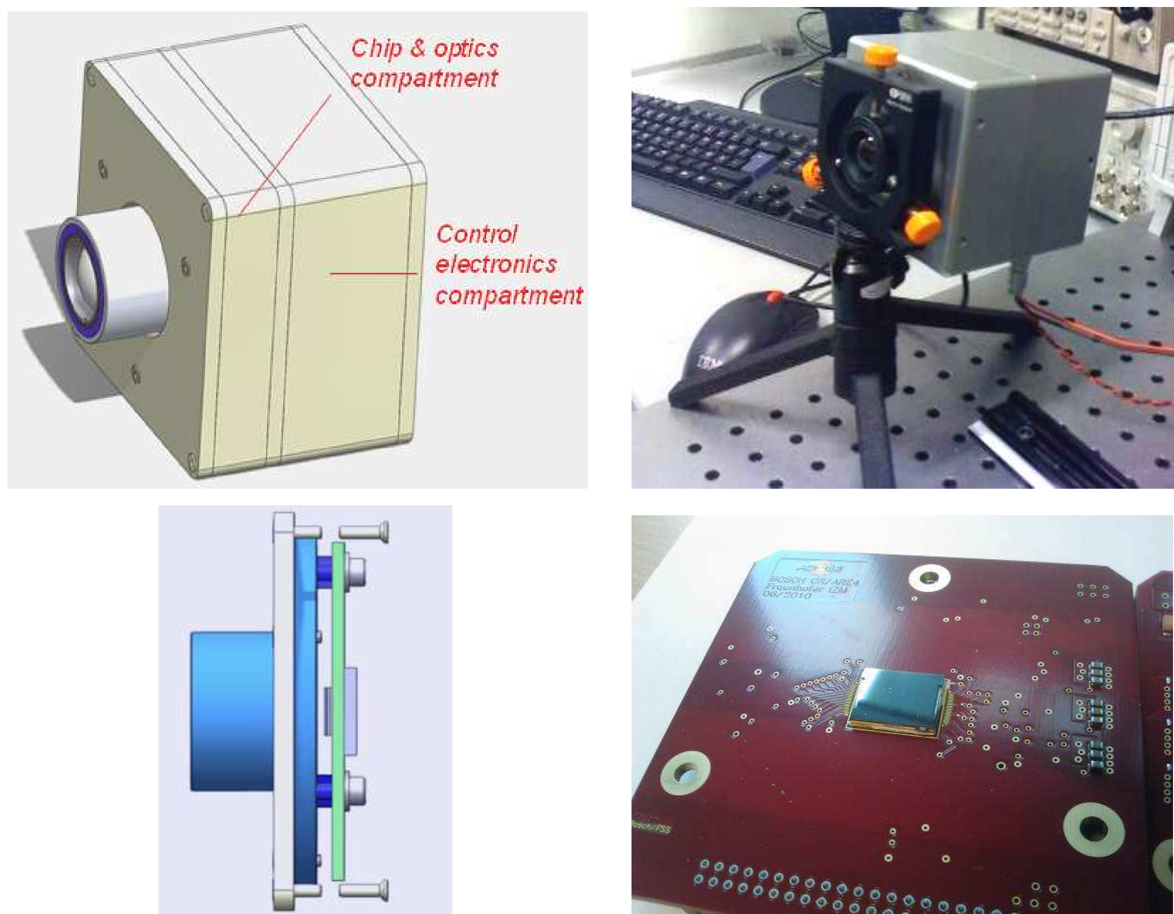

Figure 3: ADOSE FIR camera (design and prototype; top) and final setup with chip on board FIR array mounted on the lens assembly (bottom)